BASIC DIAGRAM OF CPU

Control Unit (CU)

DECODER

Cache

REGISTERS
* ACC
* MAR
* MDR
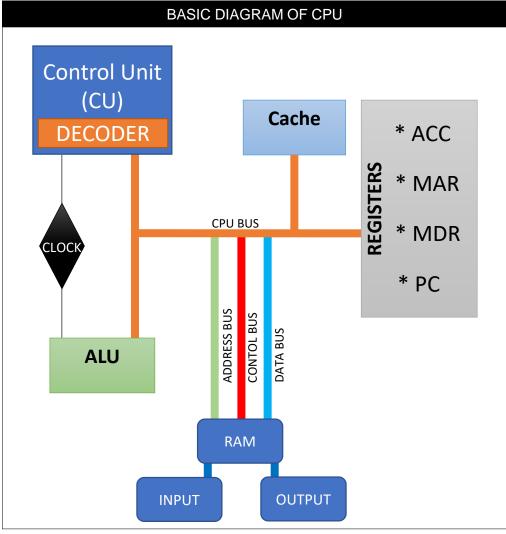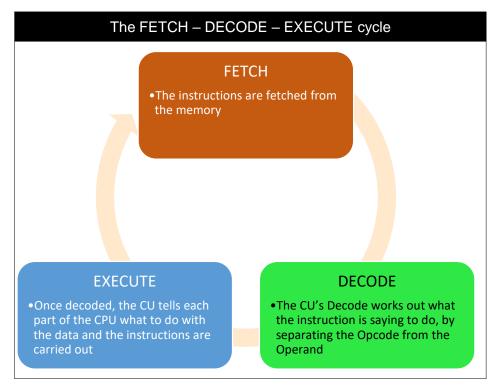* PC

CLOCK

CPU BUS

ADDRESS BUS

CONTOL BUS

DATA BUS

ALU

RAM

INPUT

OUTPUT

Multi Core Processing

Some processors have multiple CPU cores on one chip. They all have their own Level 1 cache, but share Level 2 cache, allowing them to collaborate quickly on large tasks.

CPU	CPU	CPU	CPU
L1 Cache	L1 Cache	L1 Cache	L1 Cache
L2 Cache			

The FETCH – DECODE – EXECUTE cycle

FETCH
• The instructions are fetched from the memory

EXECUTE
• Once decoded, the CU tells each part of the CPU what to do with the data and the instructions are carried out

DECODE
• The CU's Decode works out what the instruction is saying to do, by separating the Opcode from the Operand

KEY VOCABULARY

Machine Code	A program, stored in binary, that the CPU undertakes the FDE cycle on. All programs must be in machine code to work
Instruction	A single line of machine code, containing the command and data location on which it is to be executed. Stored in binary
Opcode	The first part of the instruction, is the command
Operand	The second part of the instruction is the data on which to carry out the command. This may be actual data stored in binary form, or a memory location reference of where to find the data

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